# 2-Phase IMVP-II and IMVP-III Core Controller for Mobile CPUs

# ADP3203

## FEATURES
**Pin Selectable 1- or 2-Phase Operation**
**Static and Dynamic Current Sharing Characteristics**
**Backward Compatible to IMVP-II**
**Superior Load Transient Response with ADOPT™**
  **Optimal Positioning Technology**
**Noise Blanking for Speed and Stability**
**Synchronous Rectifier Control Extends Battery Life**
**Smooth Output Transition During VID Code Change**
**Cycle-by-Cycle Current Limiting**
**Hiccup or Latched Overload Protection**
**Transient Glitch-Free Power Good**
**Soft Start Eliminates Power-On In-Rush Current Surge**
**2-Level Overvoltage and Reverse Voltage Protection**

## APPLICATIONS
**IMVP-II and IMVP-III Core DC-to-DC Converters**
**Fixed Voltage Mobile CPU Core DC-to-DC Converters**
**Notebook/Laptop Power Supplies**
**Programmable Output Power Supplies**

## GENERAL DESCRIPTION
The ADP3203 is a 1- or 2-phase hysteretic peak current dc-to-dc buck converter controller dedicated to power a mobile processor's core. The optimized low voltage design is powered from the 3.3 V system supply and draws only 10 µA maximum in shutdown. The nominal output voltage is set by a 5-bit VID code. To accommodate the transition time required by the newest processors for on-the-fly VID changes, the ADP3203 features high speed operation to allow a minimized inductor size that results in the fastest change of current to the output. To further allow for the minimum number of output capacitors to be used, the ADP3203 features active voltage positioning with ADOPT optimal compensation to ensure a superior load transient response. The output signal interfaces with the ADP3415 MOSFET driver that is optimized for high speed and high efficiency for driving both the top and bottom MOSFETs of the buck converter. The ADP3203 is capable of controlling the synchronous rectifier to extend battery lifetime in light load conditions.

## FUNCTIONAL BLOCK DIAGRAM
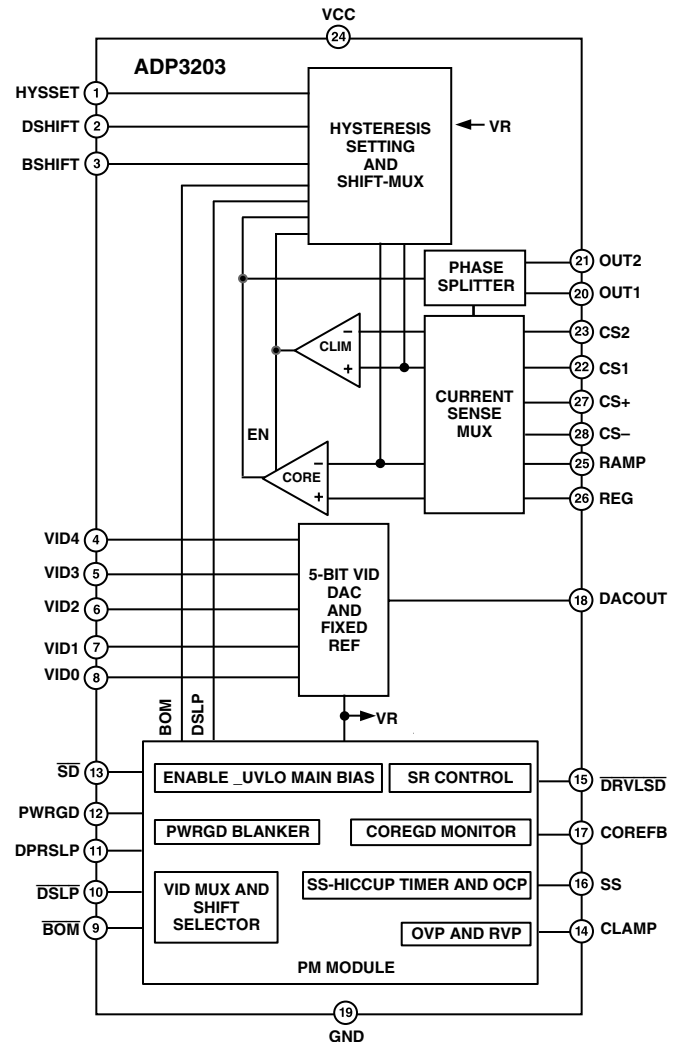


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# ADP3203–SPECIFICATIONS[1]

($0°C \leq T_A \leq 100°C$, High (H) = VCC, Low (L) = 0 V, VCC = 3.3 V, $\overline{SD}$ = H, $V_{COREFB}$ = $V_{DAC}$ (0 $V_{DACOUT}$), $V_{REG}$ = $V_{CS-}$ = $V_{VID}$ = 1.25 V, $R_{OUT1}$ =$R_{OUT2}$ = 100 kΩ, $C_{OUT1}$ = $C_{OUT2}$ = 10 pF, $C_{SS}$ =0.047 μF, $R_{PWRGD}$ = 680 Ω to 1.2 V, $R_{CLAMP}$ = 5.1 kΩ to VCC; HYSSET, BSHIFT, DSHIFT, and DPRSHIFT are open; $\overline{BOM}$ = H, DSLP = H, DPRSLP = L, unless otherwise noted.) Current sunk by a pin has a positive sign, sourced by a pin has a negative sign. Negative sign is disregarded for min and max values.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY-UVLO-SHUTDOWN** | | | | | | |
| Normal Supply Current | $I_{CC}$ | | | 7 | 9 | mA |
| UVLO Supply Current | $I_{CCUVLO}$ | VCC = 2.63 V | | | 75 | μA |
| Shutdown Supply Current | $I_{CCSD}$ | $\overline{SD}$ = L, 3.0 V ≤ VCC ≤ 3.6 V | | 10 | | μA |
| UVLO Threshold | | $\overline{SD}$ = H | | | | |
| | $V_{CCH}$ | $V_{CC}$ Ramping Up, $V_{SS}$= 0 V | | | 2.95 | V |
| | $V_{CCL}$ | $V_{CC}$ Ramping Down, | 2.65 | | | V |
| | | $V_{SS}$ Floating | | | | |
| UVLO Hysteresis | $V_{CCHYS}$ | | 50 | | | mV |
| Shutdown Threshold | | | | | | |
| (CMOS Input) | $V_{SDTH}$ | | | $V_{CC}/2$ | | V |
| **POWER GOOD** | | | | | | |
| Core Feedback Threshold Voltage | $V_{COREFBH}$ | 0.9 V < $V_{DAC}$ < 1.675 V | | | | |
| | | $V_{COREFB}$ Ramping Up | 1.12 $V_{DAC}$ | | 1.14 $V_{DAC}$ | V |
| | | $V_{COREFB}$ Ramping Down | 1.10 $V_{DAC}$ | | 1.12 $V_{DAC}$ | V |
| | | $V_{COREFB}$ Ramping Up | 0.88 $V_{DAC}$ | | 0.90 $V_{DAC}$ | V |
| | | $V_{COREFB}$ Ramping Down | 0.86 $V_{DAC}$ | | 0.88 $V_{DAC}$ | V |
| Power Good Output Voltage | $V_{PWRGD}$ | $V_{COREFB}$ = $V_{DACOUT}$ | 0.95 $V_{CC}$ | | $V_{CC}$ | V |
| (Open-Drain Output) | | $V_{COREFB}$ = 0.8 $V_{DACOUT}$ | 0 | | 0.8 | V |
| Masking Time | $t_{PWRGDMSK}$[3] | | | 100 | | μs |
| **SOFT START/HICCUP TIMER** | | | | | | |
| Charge/Discharge Current | $I_{SS}$ | $V_{SS}$ = 0 V | | −16 | | μA |
| | | $V_{SS}$ = 0.5 V | | 0.5 | | μA |
| Soft Start Enable/Hiccup | | $V_{REG}$ = 1.25 V, | | | | |
| Termination Threshold | | $V_{RAMP}$ = $V_{COREFB}$ = 1.27 V | | | | |
| | $V_{SSENDWN}$ | $V_{SS}$ Ramping Down | | 80 | 200 | mV |
| | $V_{SSENUP}$[4] | $V_{SS}$ Ramping Up | | 150 | | mV |
| Soft Start Termination/Hiccup | $V_{SSTERM}$ | $V_{RAMP}$ = $V_{COREFB}$ = 1.27 V | | | | |
| Enable Threshold | | $V_{SS}$ Ramping Up | 1.75 | 2.00 | 2.25 | V |
| **VID DAC** | | | | | | |
| VID Input Threshold | | | | | | |
| (CMOS Inputs) | $V_{VID0..4}$ | | | $V_{CC}/2$ | | V |
| VID Input Current | $I_{VID0..4}$ | VID0 to VID4 = L | | 85 | | μA |
| (Internal Active Pull-Up) | | | | | | |
| Output Voltage | $V_{DAC}$ | See VID Code, Table I | 0.600 | | 1.750 | V |
| Accuracy | $\Delta V_{DAC}/V_{DAC}$ | $0°C \leq T_A \leq 85°C$ | | | | |
| | | $1.75 \geq V_{DAC} \geq 0.850$ | −0.85 | | +0.85 | % |
| | | $0.825 \geq V_{DAC} \geq 0.600$ | −7.2 | | +7.2 | mV |
| Settling Time | $t_{DACS}$[5] | $\Delta V_{DAC}$ = 0.5 V, $C_{DAC}$ = 10 nF | | 3.5 | | μs |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CORE COMPARATOR** | | | | | | |
| Input Offset Voltage (Ramp-Reg) | $V_{COREOS}$ | $V_{REG} = 1.25$ V | | ±1 | | mV |
| Input Bias Current | $I_{REG}$, $I_{RAMP}$ | $V_{REG} = V_{RAMP} = 1.25$ V | | ±1 | | µA |
| Output Voltage | $V_{OUT\_H}$ | $V_{CC} = 3.0$ V | 2.5 | | | V |
| (OUT1, OUT2) | | | | | 3.0 | |
| | $V_{OUT\_L}$ | $V_{CC} = 3.6$ V | 0 | | 0.4 | V |
| Propagation Delay Time | $t_{RMPOUT\_PD}$[6] | $T_A = 25°C$ | | 35 | | ns |
| | | $T_A = $ Full Range | | 40 | | ns |
| Rise and Fall Time[2] | $t_{OUT\_R}$[7] | | | 7 | 10 | ns |
| | $t_{OUT\_F}$[7] | | | 7 | 10 | ns |
| Noise Blanking Time | $t_{BLNK}$ | OUT L-H Transition | | 130 | | ns |
| | | OUT H-L Transition | | 180 | | ns |
| **CURRENT LIMIT COMPARATOR** | | | | | | |
| Input Offset Voltage | $V_{CLIMOS}$ | $V_{CS-} = 1.25$ V | | ±1 | | mV |
| Input Bias Current | $I_{CS+}$, $I_{CS-}$ | $V_{CS+} = 1.25$ V | | −3 | | µA |
| Propagation Delay Time | $t_{CLiMPD}$[6] | $T_A = 25°$ C | | 60 | | ns |
| | | $T_A = $ Full Range | | 100 | | ns |
| **CURRENT SENSE MULTIPLEXER** | | | | | | |
| Transresistance | $R_{CS1-CS+}$, | Switch Is ON | | 150 | | Ω |
| | $R_{CS2-CS+}$, | Switch Is OFF | | 50 | | MΩ |
| | $R_{CS3-CS+}$ | | | | | |
| Common-Mode Voltage Range[4] | $V_{CS1} = V_{CS2}$ | | 0 | | 2 | V |
| **HYSTERESIS SETTING** | | | | | | |
| Hysteresis Current | $I_{RAMP\_H}$, | $V_{REG} = 1.25$ V | | | | |
| | $-I_{CSP\_H}$ | $V_{RAMP} = 1.23$ V, $\overline{BOM} = H$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −8 | −10 | −12 | µA |
| | | $I_{HYSSET} = -100$ µA | −85 | −100 | −115 | µA |
| | | $V_{RAMP} = 1.27$ V, $\overline{BOM} = H$ | | | | |
| | | $I_{HYSSET} = -10$ µA | 8 | 10 | 12 | µA |
| | | $I_{HYSSET} = -100$ µA | 85 | 100 | 115 | µA |
| | | $V_{RAMP} = 1.23$ V, $\overline{BOM} = L$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −6.4 | −8 | −9.6 | µA |
| | | $I_{HYSSET} = -100$ µA | −68 | −80 | −92 | µA |
| | | $V_{RAMP} = 1.27$ V, $\overline{BOM} = L$ | | | | |
| | | $I_{HYSSET} = -10$ µA | 6.4 | 8 | 9.6 | µA |
| | | $I_{HYSSET} = -100$ µA | 68 | 80 | 92 | µA |
| Hysteresis Reference Voltage | $V_{HYSSET}$ | | 1.65 | 1.7 | 1.75 | V |
| **CURRENT LIMIT SETTING** | | | | | | |
| Hysteresis Current | $I_{CS-}$ | $V_{RAMP} = 1.23$ V | | | | |
| | | $V_{REG} = V_{CS-} = V_{COREFB} = 1.25$ V | | | | |
| | | $V_{CS+} = 1.23$ V $\overline{BOM} = H$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −27 | −31.5 | −36 | µA |
| | | $I_{HYSSET} = -100$ µA | −270 | −301.5 | −333 | µA |
| | | $V_{CS+} = 1.27$ V, $\overline{BOM} = H$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −18 | −21.5 | −25 | µA |
| | | $I_{HYSSET} = -100$ µA | −180 | −201.5 | −223 | µA |
| | | $V_{CS+} = 1.23$ V, $\overline{BOM} = L$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −21 | −25.5 | −30 | µA |
| | | $I_{HYSSET} = -100$ µA | −226 | −241.5 | −267 | µA |
| | | $V_{CS+} = 1.27$ V, $\overline{BOM} = L$ | | | | |
| | | $I_{HYSSET} = -10$ µA | −14 | −17.5 | −21 | µA |
| | | $I_{HYSSET} = -100$ µA | −144 | −161.5 | −179 | µA |

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| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SHIFT SETTING** | | | | | | |
| Battery Shift Current | $I_{RAMPB}$, $I_{CS+B}$ | $V_{VID}$ = 1.25 V, $I_{BSHIFT}$ = −100 μA, $\overline{BOM}$ = L, DSLP = H | −92.5 | −100 | −107.5 | mA |
| Battery Shift Reference Voltage | $V_{BSHIFT}$ | | | $V_{DAC}$ | | V |
| Deep Sleep Shift Current | $I_{RAMPD}$, $I_{CS+D}$ | $V_{VID}$ = 1.25 V, $I_{DSHIFT}$ = −100 μA, $\overline{BOM}$ = H, DSLP = L | −92.5 | −100 | −107.5 | mA |
| Deep Sleep Shift Reference Voltage | $V_{DSHIFT}$ | | | $V_{DAC}$ | | V |
| **SHIFT CONTROL INPUTS** | | | | | | |
| BOM Threshold (CMOS Input) | $V_{BOM}$ | | | $V_{CC}/2$ | | V |
| DSLP Threshold ($V_{TT}$-Level CMOS Input) | $V_{DSLP}$ | | | 0.9 | | V |
| DPRSLP Mode Threshold[8] (CMOS Input) | $V_{DPRSLP}$ | | | $V_{CC}/2$ | | V |
| **LOW SIDE DRIVE CONTROL** | | | | | | |
| Output Voltage (CMOS Output) | $V_{DRVLSD}$ | DPRSLP = H | 0 | | 0.4 | V |
| | | DPRSLP = L | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| Output Current | $I_{DRVLSD}$ | DPRSLP = H, $V_{DRVLSD}$ = 1.5 V | 0.4 | | | mA |
| | | DPRSLP = L, $V_{DRVLSD}$ = 1.5 V | −0.4 | | | mA |
| **OVER/REVERSE VOLTAGE PROTECTION-CORE FEEDBACK** | | | | | | |
| Overvoltage Threshold | $V_{COREFB,OVP}$ | $V_{COREFB}$ Rising | | 2.0 | | V |
| Reverse Voltage Threshold | $V_{COREFB,OVP}$ | $V_{COREFB}$ Falling | | −0.3 | | V |
| Output Voltage (Open-Drain Output) | $V_{CLAMP}$ | | 0.7 $V_{CC}$ | | $V_{CC}$ | V |
| Output Current | $I_{CLAMP}$ | $V_{COREFB}$ = 2.2 V, $V_{CLAMP}$ = 5 V | | | 10 | μA |
| | | $V_{COREFB}$ = $V_{DAC}$, $V_{CLAMP}$ = 5 V | 2 | 4 | | mA |

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]Guaranteed by characterization.

[3]Two test conditions: 1)PWRGD is OK but forced to fail by applying an out-of-the-Core-Good-window voltage ($V_{COREFB,BAD}$ = 1.0 V at $V_{VID}$ = 1.25 V setting) to the COREFB pin right after the moment that $\overline{BOM}$ or DPRSLP is asserted/deasserted. PWRGD should not fail immediately, only with the specified blanking delay time. 2) PWRGD is forced to fail ($V_{COREFB, BAD}$ = 1.0 V at $V_{VID}$ = 1.25 V setting) but gets into the Core Good window ($V_{COREFB, GOOD}$ = 1.25 V) right after the moment that $\overline{BOM}$ or DPRSLP is asserted/deasserted. PWRGD should not go high immediately, only with the specified blanking delay time.

[4]Guaranteed by design.

[5]Measured from 50% of VID code transition amplitude to the point where $V_{DACOUT}$ settles within ±1% of its steady state value.

[6]40 mVp-p amplitude impulse with 20 mV overdrive. Measured from the input threshold intercept point to 50% of the output voltage swing.

[7]Measured between the 30% and 70% points of the output voltage swing.

[8]DPRSLP circuit meets the minimum 30 ns DPRSLPVR signal assertion requirement; guaranteed by design.

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## ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage (VCC) . . . . . . . . . . . . . . . −0.3 V to +7 V
All Other Inputs/Outputs . . . . . . . . . . . −0.3 V to VCC + 0.3 V
Operating Ambient Temperature Range . . . . . . 0°C to 100°C
Junction Temperature Range . . . . . . . . . . . . . . 0°C to 150°C
$\theta_{JA}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 98°C/W
Storage Temperature Range . . . . . . . . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . . . . . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.
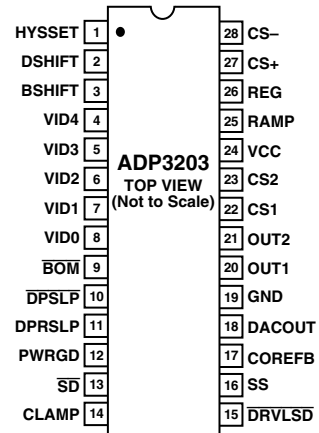
### ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADP3203JRU-0.85-RL | 0.85 V | 0°C to 100°C | TSSOP-28 |
| ADP3203JRU-0.85-R7 | 0.85 V | 0°C to 100°C | TSSOP-28 |
| ADP3203JRU-1.0-RL | 1 V | 0°C to 100°C | TSSOP-28 |
| ADP3203JRU-1.0-RL7 | 1 V | 0°C to 100°C | TSSOP-28 |

### PIN CONFIGURATION

| Left Pins | | Right Pins |
|---|---|---|
| HYSSET | 1 | 28 CS− |
| DSHIFT | 2 | 27 CS+ |
| BSHIFT | 3 | 26 REG |
| VID4 | 4 | 25 RAMP |
| VID3 | 5 | 24 VCC |
| VID2 | 6 | 23 CS2 |
| VID1 | 7 | 22 CS1 |
| VID0 | 8 | 21 OUT2 |
| $\overline{BOM}$ | 9 | 20 OUT1 |
| $\overline{DPSLP}$ | 10 | 19 GND |
| DPRSLP | 11 | 18 DACOUT |
| PWRGD | 12 | 17 COREFB |
| $\overline{SD}$ | 13 | 16 SS |
| CLAMP | 14 | 15 $\overline{DRVLSD}$ |

ADP3203 TOP VIEW (Not to Scale)

**Table I. VID Code**

| VID4 | VID3 | VID2 | VID1 | VID0 | VOUT |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1.750 |
| 0 | 0 | 0 | 0 | 1 | 1.700 |
| 0 | 0 | 0 | 1 | 0 | 1.650 |
| 0 | 0 | 0 | 1 | 1 | 1.600 |
| 0 | 0 | 1 | 0 | 0 | 1.550 |
| 0 | 0 | 1 | 0 | 1 | 1.500 |
| 0 | 0 | 1 | 1 | 0 | 1.450 |
| 0 | 0 | 1 | 1 | 1 | 1.400 |
| 0 | 1 | 0 | 0 | 0 | 1.350 |
| 0 | 1 | 0 | 0 | 1 | 1.300 |
| 0 | 1 | 0 | 1 | 0 | 1.250 |
| 0 | 1 | 0 | 1 | 1 | 1.200 |
| 0 | 1 | 1 | 0 | 0 | 1.150 |
| 0 | 1 | 1 | 0 | 1 | 1.100 |
| 0 | 1 | 1 | 1 | 0 | 1.050 |
| 0 | 1 | 1 | 1 | 1 | 1.000 |
| 1 | 0 | 0 | 0 | 0 | 0.975 |
| 1 | 0 | 0 | 0 | 1 | 0.950 |
| 1 | 0 | 0 | 1 | 0 | 0.925 |
| 1 | 0 | 0 | 1 | 1 | 0.900 |
| 1 | 0 | 1 | 0 | 0 | 0.875 |
| 1 | 0 | 1 | 0 | 1 | 0.850 |
| 1 | 0 | 1 | 1 | 0 | 0.825 |
| 1 | 0 | 1 | 1 | 1 | 0.800 |
| 1 | 1 | 0 | 0 | 0 | 0.775 |
| 1 | 1 | 0 | 0 | 1 | 0.750 |
| 1 | 1 | 0 | 1 | 0 | 0.725 |
| 1 | 1 | 0 | 1 | 1 | 0.700 |
| 1 | 1 | 1 | 0 | 0 | 0.675 |
| 1 | 1 | 1 | 0 | 1 | 0.650 |
| 1 | 1 | 1 | 1 | 0 | 0.625 |
| 1 | 1 | 1 | 1 | 1 | 0.600 |

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| Pin | Mnemonic | Function |
|-----|----------|----------|
| 1 | HYSSET | Hysteresis Set. This is an analog I/O pin whose output is a fixed voltage reference and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set the hysteretic currents for the core comparator and the current limit comparator. Modification of the resistance will affect both the hysteresis of the feedback regulation and the current limit set-point and hysteresis. |
| 2 | DSHIFT | Deep Sleep Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input is a current that is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{DPSLP}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to Deep Sleep Mode of CPU operation. The use of the VID code as the reference makes the deep sleep offset a fixed percentage of the VID setting, as required by specifications. |
| 3 | BSHIFT | Battery Optimized Mode ($\overline{\text{BOM}}$) Shift. This is an analog I/O pin whose output is the VID reference voltage and whose input current is programmed by an external resistance to ground. The current is used in the IC to set a switched bias current out of the RAMP pin, depending on whether it is activated by the $\overline{\text{BOM}}$ signal. When activated, this added bias current creates a downward shift of the regulated core voltage to a predetermined optimum level for regulation corresponding to the Battery Optimized Mode of the CPU operation. The use of the VID code as the reference makes the BSHIFT a fixed percentage of the VID setting, as required by specifications. |
| 4–8 | VID[4:0] | Voltage Identification Inputs. These are the VID inputs for logic control of the programmed reference voltage that appears at the DACOUT pin, and via external component configuration, is used for setting the output voltage regulation point. The VID pins have a specified internal pull-up current that, if left open, will default the pins to a logic high state. The VID code does not set the DAC output voltage directly but through a transparent latch that is clocked by the $\overline{\text{BOM}}$ pin's GMUXSEL signal rising and falling edge. |
| 9 | $\overline{\text{BOM}}$ | Battery Optimized Mode Control (Active Low). This digital input pin corresponds to the system's GMUXSEL signal, which corresponds to Battery Optimized Mode of the CPU operation in its active low state and Performance Optimized Mode (POM) in its deactivated high state. The signal also controls the optimal positioning of the core voltage regulation level by offsetting it downward in Battery Optimized Mode according to the functionality of the BSHIFT and RAMP pins. It is also used to initiate a masking period for the PWRGD signal whenever a GMUXSEL signal transition occurs. |
| 10 | $\overline{\text{DPSLP}}$ | Deep Sleep Mode Control (Active Low). This is a digital input pin corresponding to the system's $\overline{\text{STP CPU}}$ signal that, in its active state, corresponds to Deep Sleep Mode of the CPU operation, which is a subset operating mode of either $\overline{\text{BOM}}$ or POM operation. The signal controls the optimal positioning of the core voltage regulation level by offsetting it downward according to the functionality of the DSHIFT and RAMP pins. |
| 11 | DPRSLP | Deeper Sleep Mode Control (Active High). This is a digital input pin corresponding to the system's DPRSLPVR signal corresponding to Deeper Sleep Mode of the CPU operation. When the signal is activated, it controls the DAC output voltage by disconnecting the VID signals from the DAC input and setting a specified internal deeper sleep code instead. At deassertion of the DPRSLPVR signal, the DAC output voltage returns to the voltage level determined by the external VID code. The DPRSLPVR signal is also used to initiate a blanking period for the PWRGD signal to disable its response to a pending dynamic core voltage change that corresponds to the VID code transition. |

**PIN FUNCTION DESCRIPTIONS (continued)**

| Pin | Mnemonic | Function |
|-----|----------|----------|
| 12 | PWRGD | Power Good (Active High). This open-drain output pin, via the assistance of an external pull-up resistor to the desired voltage, indicates that the core voltage is within the specified tolerance of the VID programmed value, or else is in a VID transition state as indicated by a recent state transition of either the $\overline{BOM}$ or DPRSLP pins. PWRGD is deactivated (pulled low) when the IC is disabled, in UVLO Mode, or starting up, or the COREFB voltage is out of the core Power Good window. The open-drain output allows external wired ANDing (logical NORing) with other open-drain/collector Power Good indicators. |
| 13 | $\overline{SD}$ | Shutdown (Active Low). This is a digital input pin coming from a system signal that, in its active state, shuts down the IC operation, placing the IC in its lowest quiescent current state for maximum power savings. |
| 14 | CLAMP | Clamp (Active High). This open-drain output pin, via the assistance of an external pull-up resistor, indicates that the core voltage should be clamped for its protection. To allow the highest level of protection, the CLAMP signal is developed using both a redundant reference and a redundant feedback path with respect to those of the main regulation loop. The signal is timed out using the soft start capacitor, so an external current protection mechanism (e.g., a fuse or ac adapter's current limit) should be tripped within ~3 times the programmed soft start time (e.g., 5 ms~10 ms). In a preferred and more conservative configuration, the core voltage is clamped by an external FET. The initial protection function is served when it is activated by detection of either an overvoltage or a reverse voltage condition on the COREFB pin. Due to loss of the latched signal at IC power-off, backup protection function is served by connecting the pull-up resistor to a system "ALWAYS" regulator output (e.g., V5_ALWAYS). If the external FET is used, this implementation will keep the core voltage clamped until the ADP3203 has power reapplied, thus keeping protection for the CPU even after a hard-failure power-down and restart (e.g., a shorted top or bottom FET). |
| 15 | $\overline{DRVLSD}$ | Drive-Low Shutdown (Active Low). In its active state, this digital output pin indicates that the lower FET of the core VR should be disabled. In the suggested application schematic, this pin is directly connected to the pin of the same name on the ADP3415 or other driver IC. Drive-low shutdown is normally activated by the DPRSLP signal corresponding to a light load condition, but a number of dynamic conditions can override the control of this pin as needed. |
| 16 | SS | Soft Start. The output of this analog I/O pin is a controlled current source used to charge or discharge an external grounded capacitor; the input is the detected voltage that is indicative of elapsed time. The pin controls the soft start time of the IC as well as the hiccup cycle time during overload, including but not limited to short circuit, overvoltage, and reverse voltage. Hiccup operation was added to reduce short circuit power dissipation by more than an order of magnitude, while still allowing an automatic restart when the failure mode ceased. |
| 17 | COREFB | Core Feedback. This high impedance analog input pin is used to monitor the output voltage for setting the proper state of the PWRGD and CLAMP pins. It is generally recommended to RC-filter the ripple and noise from the monitored core voltage, as suggested by the application schematic. |
| 18 | DACOUT | Digital-to-Analog Converter Output. This output voltage is the VID-controlled reference voltage whose primary function is to determine the output voltage regulation point. |
| 19 | GND | Ground |
| 20 | OUT1 | Output to Driver 1. This digital output pin is used to command the state of the switched node via the driver and MOSFET switches. It should be connected to the IN pin of the ADP3415 driver that corresponds to the first of two channels. |

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| Pin | Mnemonic | Function |
|---|---|---|
| 21 | OUT2 | Output to Driver 2. This digital output pin is used to command the state of the switched node via the driver. It should be connected to the IN pin of the ADP3415 driver that corresponds to the second of two channels. |
| 22 | CS1 | Current Sense, Channel 1. This high impedance analog input pin is used to provide negative feedback of the current information for the first of two channels. |
| 23 | CS2 | Current Sense, Channel 2. This high impedance analog input pin is used to provide negative feedback of the current information for the second of two channels. The pin is also used to determine whether the chip is acting as a single- or dual-phase controller. If the pin is tied to VCC but not a sense resistor, then the dual-phase operation is disabled; the chip works as a single-phase controller. In this condition, the second phase's output signal (OUT2) does not switch but stays static low. |
| 24 | VCC | Power Supply. This should be connected to the system's 3.3 V power supply output. |
| 25 | RAMP | Regulation Ramp Feedback Input. The RAMP pin voltage is compared against the REG pin for cycle-by-cycle switching response. Several switched current sources also appear at this input: the cycle-by-cycle hysteresis setting switched current programmed by the HYSSET pin, the BOM shift current programmed by the BSHIFT pin, and the Deep Sleep shift current programmed by the DSHIFT pin. The external resistive termination at this pin sets the magnitude of the hysteresis applied to the regulation loop. |
| 26 | REG | Regulation Voltage Summing Input. This is a high impedance analog input pin into which the voltage reference of the feedback loop allows the summing of both the DACOUT voltage and the core voltage for programming the output resistance of the core voltage regulator. This is also the pin at which an optimized transient response can be tailored using Analog Devices' patented ADOPT design technique. |
| 27 | CS+ | Current Limit Positive Sense. This high impedance analog input pin is multiplexed between either of the two current-sense inputs during the high state of the OUT pin of the respective channel. During the common off-time of both channels, the pin's voltage reflects the average of the two channels. The multiplexed current sense signal is passed to the core comparator through an external resistive termination connected from this pin to the RAMP pin. The external (RAMP) resistor sets the magnitude of the hysteresis applied to the regulation loop. |
| 28 | CS– | Current Limit Negative Sense. This high impedance analog input pin is normally Kelvin connected to the negative node of the current sense resistor(s) via a current-limit programming resistor. A hysteretically controlled current—three times the current programmed at the HYSSET pin—also flows out of this pin and develops a current-limit setting voltage across that resistor, which must then be matched by the inductor current flowing in the current sensing resistor in order to trigger the current limit function. When triggered, the current flowing out of this pin is reduced to two-thirds of its previous value, producing hysteresis in the current limiting function. |
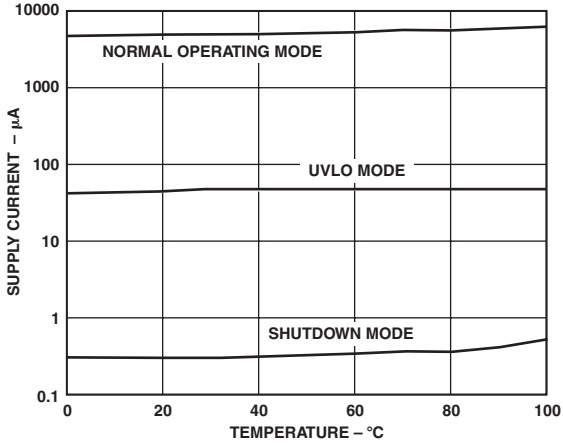
TPC 1. Supply Current vs. Temperature



TPC 2. DAC Output Voltage vs. Temperature



TPC 3. DAC Output Voltage vs. Temperature
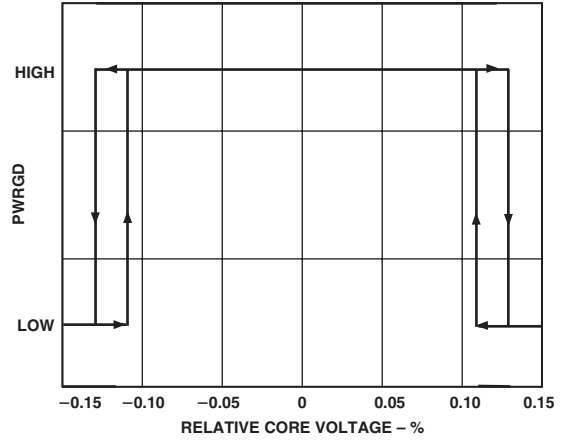


TPC 4. Power Good vs. Relative Core Voltage Variation
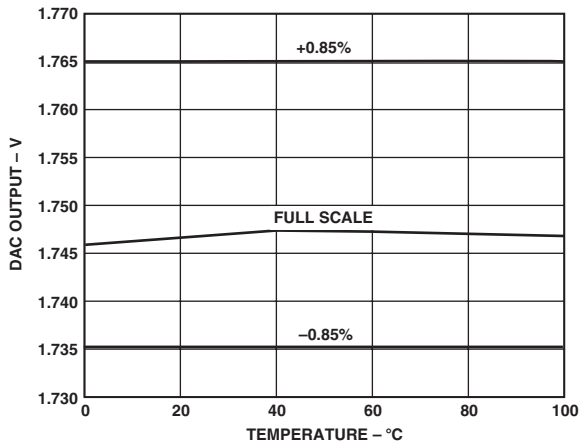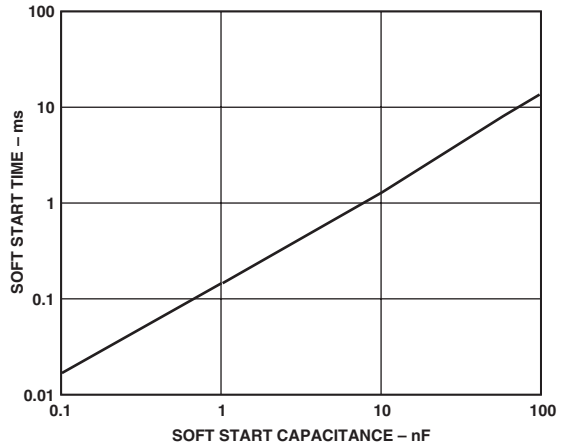


TPC 5. Soft Start Timing vs. Timing Capacitor
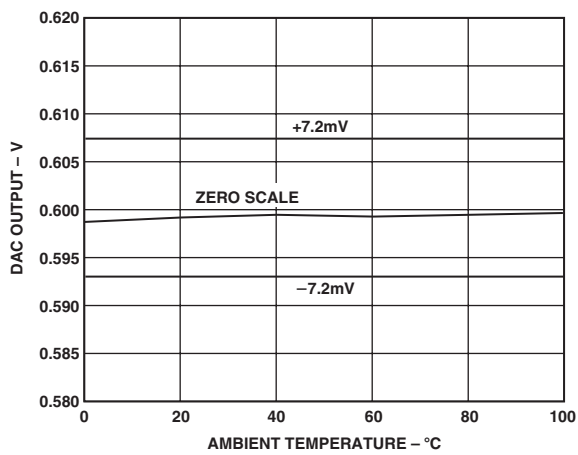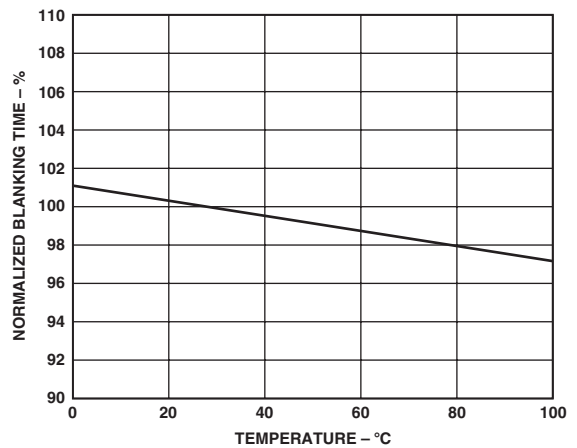


TPC 6. PWRGD Blanking Time vs. Temperature
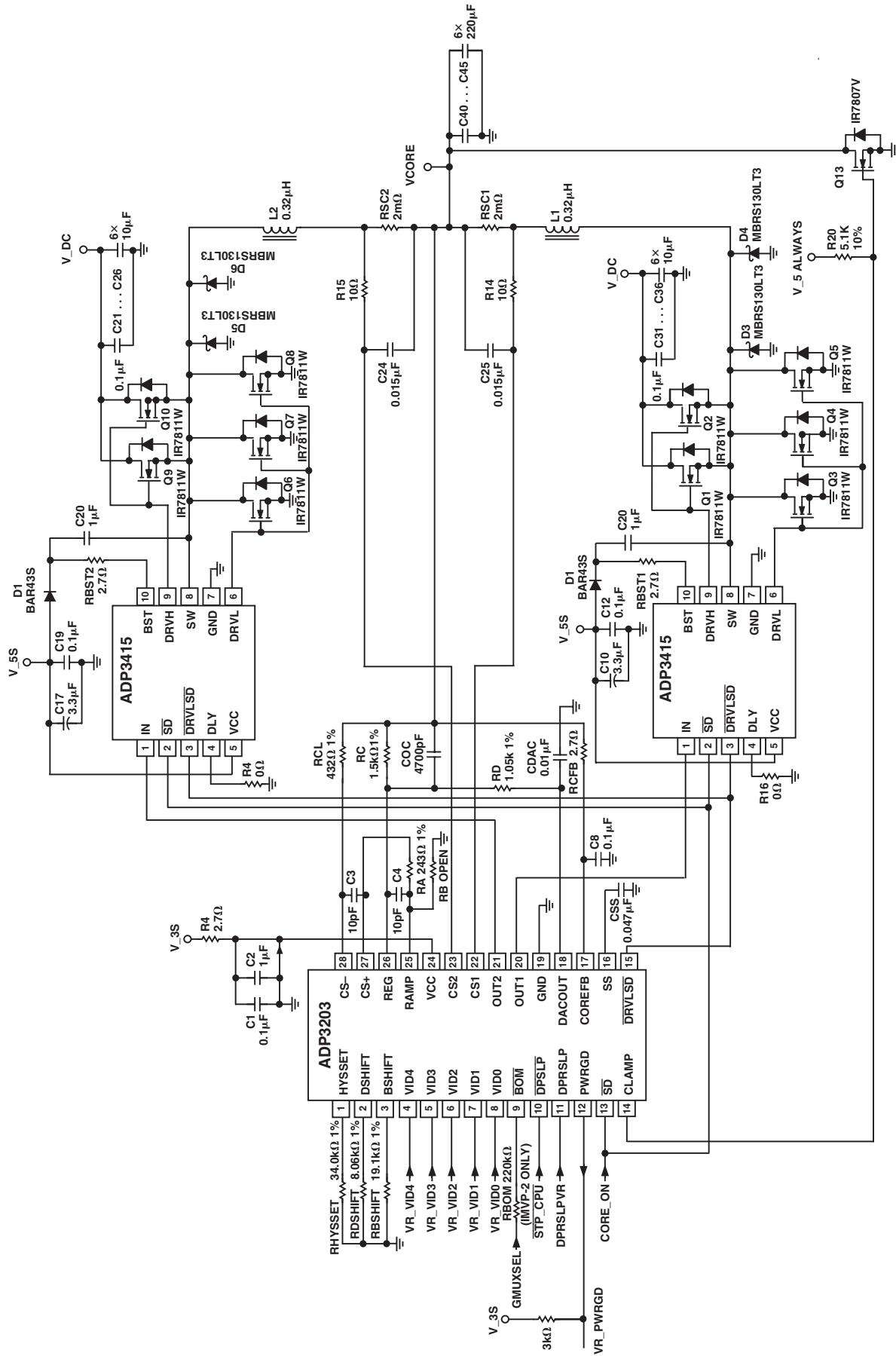Normalized to 25°C

# ADP3203



*Figure 1.  Typical Application*

## THEORY OF OPERATION

### Overview

Featuring a new proprietary single- or dual-channel buck converter hysteretic control architecture developed by Analog Devices, the ADP3203 is the optimal core voltage control solution for both IMVP-II and IMVP-III generation microprocessors. The complex, multitiered regulation requirements of either IMVP specification are easily implemented with the highly integrated functionality of this controller.

### Power Conversion Control Architecture

Driving of the individual channels is accomplished using external drivers, such as the ADP3415. One PWM interface pin per channel, OUT1 and OUT2, is provided. A separate pin, $\overline{DRVLSD}$, commands the driver to enable or disable synchronous rectifier operation during the off time of each channel. The same $\overline{DRVLSD}$ pin is connected to all three drivers.

The ADP3203 uses hysteretic control. The resistor from the HYSSET Pin to ground sets up a current that is switched bidirectionally into a resistor interconnected between the RAMP and CS+ pins. The switching of this current sets the hysteresis.

In its dual-channel configuration, the hysteretic control requires multiplexing information in all channels. The inductor current of the channel that is driven high is controlled against the upper hysteresis limit. During the common off time of the channels, the inductor currents are averaged together and compared against the lower hysteresis limit. This proprietary off-time averaging technique serves to eliminate a systematic offset that otherwise appears in a fully multiplexed hysteretic control system.

### Compensation

As with all ADI products for core voltage control, the controller is compatible with ADOPT compensation, which provides the optimum output voltage containment within a specified voltage window or along a specified load line using the fewest possible output capacitors. The inductor ripple current is kept at a fixed programmable value, while the output voltage is regulated with fully programmable voltage positioning parameters, which can be tuned to optimize the design for any particular CPU regulation specification. By controlling the ripple current rather than the ripple voltage, the frequency variations associated with changes in output impedance for standard ripple regulators will not appear.

### Feedback/Current Sensing

Accurate current sensing is needed to accomplish output voltage positioning accurately, which, in turn, is required to allow the minimum number of output capacitors to be used to contain transients. A current sense resistor is used between each inductor and the output capacitors. To allow the control to operate without amplifiers, the negative feedback signal is multiplexed from the inductor or upstream side of the current sense resistors, and a positive feedback signal, if needed for load line tuning, is taken from the output or downstream side.

### Output Voltage Programming by VID, Offsets, and Load Line

In the IMVP-II and IMVP-III specifications, the output voltage is a function of both the core current (according to a specified load line) and the system operating mode (i.e., performance or battery optimized, normal or deep sleep clocking state, or deeper sleep). The VID code programs the "nominal" core voltage. The core voltage decreases as a function of load current along the load line, which is synonymous with an output resistance of the power converter. The core voltage is also offset by a dc value—usually specified as a percentage—depending on the operating mode. The voltage offset is also called a "shift."

Two pins, BSHIFT and DSHIFT, are used to program the magnitude of the voltage shifts. The voltage shifts are accomplished by injecting current at the node of the negative input pin of the feedback comparator. Resistive termination at the pins determines the magnitude of the voltage shifts.

Two other pins, $\overline{BOM}$ and $\overline{DPSLP}$, are used to activate the respective two shifts only in their active low states. In the ADP3203, the shifts are mutually exclusive, with the deep sleep shift (controlled by the $\overline{DPSLP}$ and DSHIFT pins) being the dominant one. Another pin, DPRSLP, eliminates both shifts only in its active high state. Its assertion corresponds to the Deeper Sleep Operating Mode.

### Current Limiting

The current programmed at the HYSSET pin and a resistor from the CS– pin to the common node of the current sense resistors set the current limit. If the current limit threshold is triggered, a hysteresis is applied to the threshold so that hysteretic control is maintained during a current limited operating mode.

### Soft Start and Hiccup

A capacitor from the SS pin to ground determines both the soft start time and the frequency at which hiccup will occur under a continuous short circuit or overload.

### System Signal Interface

Several pins of the ADP3203 are meant to connect directly to system signals. The VID pins connect to the system VID control signals. The DPRSLP pin connects to the system's DPRSLPVR signal. The $\overline{DPSLP}$ pin connects to the system's $\overline{DPSLP}$ or STPCPU signal. The $\overline{BOM}$ signal connects to the system's GMUXSEL signal. In an IMVP-II system, the GMUXSEL signal precedes any VID code change with a few nanoseconds, while in an IMVP-III system, it follows it with a maximum 12 µs delay. To comply with both specifications, the ADP3203 has a VID register in front of the DAC inputs that is written by a short pulse generated at the rising or falling edge of the GMUXSEL signal. In an IMVP-II configuration, if the external VID multiplex settling time is longer than the internal VID register's write pulsewidth, then the insertion of an external RC delay network in the GMUXSEL signal path (in front of the $\overline{BOM}$ pin) is recommended. The Intel specification calls for maximum 200 ns VID code setup time. This specification can be met with a simple RC network that consists of only a 220 kΩ resistor and no external capacitor, just the $\overline{BOM}$ pin's capacitance.

### Undervoltage Lockout

The ADP3203's supply pin, VCC, has undervoltage lockout (UVLO) functionality to ensure that if the supply voltage is too low to maintain proper operation, the IC will remain off and in a low current state.

### Overvoltage Protection (OVP) and Reverse Voltage Protection (RVP)

The ADP3203 features a comprehensive redundantly monitored OVP and RVP implementation to protect the CPU core against an excessive or reverse voltage, e.g., as might be induced by a component or connection failure in the control or power stage.

# ADP3203

Two pins are associated with the OVP/RVP circuitry—a pin for output voltage feedback, COREFB, which is also used for Power Good monitoring but not for voltage regulation, and an output pin, CLAMP.

The CLAMP pin defaults to a low state at startup of the ADP3203 and remains low until an overvoltage or reverse voltage condition is detected. If either condition is detected, the CLAMP pin is switched and latched to the VCC pin. The high state of the CLAMP pin is reset only after several milliseconds as the soft start pin discharges.

For maximum and fastest protection, the CLAMP pin should be used to drive the gate of a power MOSFET whose drain source is connected across the CPU core voltage. Detection of overvoltage or reverse voltage will clamp the core voltage to essentially zero, thus quickly removing the fault condition and preventing further energy from being applied to the CPU core.

For a less comprehensively protective but also less costly solution, the CLAMP pin may be used to latch the disconnection of input power. The latch should be powered whenever any input power source is present. Typically, such a latching circuit is already present in a system design, so it becomes only a matter of allowing the CLAMP pin to also trigger the latch. In this configuration, the latched off state of the system would be indicative of a system failure. The overvoltage/reverse voltage protective means is via not allowing the continued application of energy to the CPU core. The design objective should be, however, to ensure that the CPU core could safely absorb the remaining energy in the power converter, since this energy is not clamped as in the preferred configuration.

## LAYOUT CONSIDERATIONS

### Advantages in PCB Layout

This 2-phase solution separates the controller (ADP3203) and the MOSFET drivers (ADP3415). Today, most motherboards only leave small pieces of PCB area for the power management circuit. Therefore, the separation of the controller and the MOSFET drivers gives much greater freedom in layout than any single chip solution.

Meanwhile, the separation also provides the freedom to place the analog controller in a relatively quiet area in the motherboard. This can minimize the susceptibility of the controller to injected noise. Any single-chip solution with a high speed loop design will suffer larger susceptibility to jitter that appears as modulation of the output voltage.

The ADP3203 maximizes the integration of IMVP-III features. Therefore, no additional externally implemented functions are required to comply with IMVP-III specifications. This saves PCB area for component placement on the motherboard.

### PCB Layout Consideration for ADP3203/ADP3415

The following guidelines are recommended for optimal performance of the ADP3203 and ADP3415 in a power converter. The circuitry is considered in three parts: the power switching circuitry, the output filter, and the control circuitry.

### Placement Overview

1. For ideal component placement, the output filter capacitors will divide the power switching circuitry from the control section. As an approximate guideline considered on a single-sided PCB, the best layout would have components aligned in the following order: ADP3415, MOSFETs and input capacitor, output inductor, current sense resistor, output capacitors, control components, and ADP3203. Note that the ADP3203 and ADP3415 are completely separated for an ideal layout, which is impossible with a single-chip solution. This keeps the noisy switched power section isolated from the precision control section and gives more freedom in the layout of the power switching circuitry.

2. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad if possible and immediately surrounding it, is recommended. Two important reasons for this are: improvement of the current rating through the vias (if it is a current path) and improved thermal performance, especially if there is opportunity to spread the heat with a plane on the opposite side of the PCB.

### Power Switching Circuitry

### ADP3415, MOSFETs, and Input Capacitors

3. Locate the ADP3415 near the MOSFETs so that the loop inductance in the path of the top gate drive returned to the SW pin is small, and similarly for the bottom gate drive whose return path is the ground plane. The GND pin should have at least one very close via into the ground plane.

4. Locate the input bypass MLC capacitors close to the MOSFETs so that the physical area of the loop enclosed in the electrical path through the bypass capacitor and around through the top and bottom MOSFETs (drain source) is small and wide. This is the switching power path loop.

5. Make provisions for thermal management of all the MOSFETs. Heavy copper and wide traces to ground and power planes will help to pull the heat out. Heatsinking by a metal tap soldered in the power plane near the MOSFETs will help. Even just a small airflow can help tremendously. Paralleled MOSFETs to achieve a given resistance will help spread the heat.

6. An external Schottky diode (across the bottom MOSFET) may increase efficiency by a small amount (< ~1%), depending on its forward voltage drop compared to the MOSFET's body diode at a given current; a MOSFET with a built-in Schottky is more effective. For an external Schottky, it should be placed next to the bottom MOSFET or it may not be effective at all.

7. The VCC bypass capacitor should be close to the VCC pin and connected on either a very short trace to the GND pin or to the GND plane.

### Output Filter

### Output Inductor and Capacitors, Current Sense Resistor

8. Locate the current sense resistors very near to the output voltage plane.

9. The load-side heads of sense resistors should join as closely as possible for accurate current signal measurement of each phase.

10. PCB trace resistances from the current sense resistors to the regulation point should be minimized, known (calculated or measured), and compensated for as part of the design if it is significant. (Remote sensing is not sufficient

for relieving this requirement.) A square section of 1-ounce copper trace has a resistance of ~500 μΩ that adds to the specified dc output resistance of the power converter. The output capacitors should similarly be close to the regulation point and well tied into power planes as impedance here will add to the ac output resistance (i.e., the ESR) that is implicitly specified as well.

11. Whenever high currents must be routed between PCB layers, vias should be used liberally to create parallel current paths so that the resistance and inductance are minimized and the via current rating is not exceeded.

**Control Circuitry**

*ADP3203, Control Components*

12. If the ADP3203 cannot be placed as previously recommended, care should be taken to keep the device and surrounding components away from radiation sources (e.g., from power inductors) and capacitive coupling from noisy power nodes.

13. Noise immunity can be improved by the use of a devoted signal ground plane for the power controller and its surrounding components. Space for a ground plane might readily be available on a signal plane of the PCB since it is often unused in the vicinity of the power controller.

14. If critical signal lines (i.e., signals from the current sense resistor leading back to the ADP3203) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals.

15. Absolutely avoid crossing any signal lines over the switching power path loop, described previously.

16. Accurate voltage positioning depends on accurate current sensing, so the control signals that monitor the voltage differentially across the current sense resistor should be Kelvin-connected. Please refer to the ADI Evaluation Board of the ADP3203 and its documentation for control signal connection with sense resistors.

17. The RC filter used for the current sense signal should be located near the control components as this serves the dual purpose of filtering out the effect of the current sense resistors' parasitic inductance and the noise picked up along the routing of the signal. The former purpose is achieved by having the time constant of the RC filters approximately matched to that of the sense resistors and is important for maintaining the accuracy of the current signal.

## APPLICATION INFORMATION

**Theoretical Background**

This application section presents the theoretical background for multiphase dc-to-dc converters using the ADP320x family of controllers for mobile CPUs. Members of that family control multiphase ripple regulators (also called hysteretic regulators) in a configuration that allows employing ADOPT, Analog Devices' optimal voltage positioning technique, to implement the desired output voltage and load line both statically and dynamically, as required by Intel's IMVP-II and IMVP-III specifications.

**Single-Phase Hysteretic Regulator with ADOPT**

Figure 2 shows the conventional single-phase hysteretic regulator and the characteristic waveforms. The operation is as follows. During the time the upper transistor, Q1, is turned on, the inductor current, $I_L$, and also the output voltage, $V_{OUT}$, increase. When $V_{OUT}$ reaches the upper threshold of the hysteretic comparator, Q1 is turned off, Q2 is turned on, and the inductor current and the output voltage decrease. The cycle repeats after $V_{OUT}$ reaches the lower threshold of the hysteretic comparator.
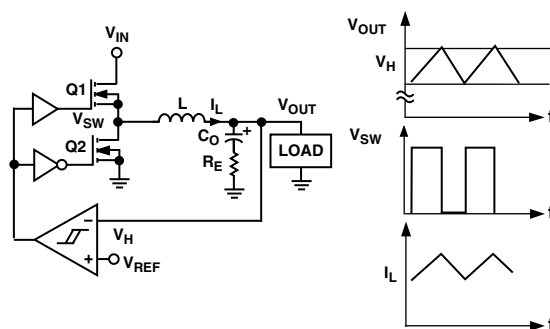


*Figure 2. Conventional Hysteretic Regulator and Its Characteristic Waveforms*

Since there is no voltage error amplifier in the hysteretic regulator, its response to any change in the load current or the input voltage is virtually instantaneous. Therefore, the hysteretic regulator represents the fastest possible dc-to-dc converter. A slight disadvantage of the conventional hysteretic regulator is that its frequency varies with the input and output voltages. In a typical mobile CPU converter application, the worst-case frequency variation due to the input voltage variation is in the order of 30%, which is usually acceptable. In the simplest implementation of the hysteretic converter, shown in Figure 2, the frequency also varies proportionally with the ESR, $R_E$, of the output capacitor. Since the initial value is often poorly controlled, and the ESR of electrolytic capacitors also changes with temperature and age, practical ESR variations can easily lead to a frequency variation in the order of three to one. However, a modification of the hysteretic topology eliminates the dependence of the operating frequency on the ESR. In addition, the modification allows the optimal implementation, ADOPT, of Intel's IMVP-II and IMVP-III load line specifications. Figure 3 shows the modified hysteretic regulator.
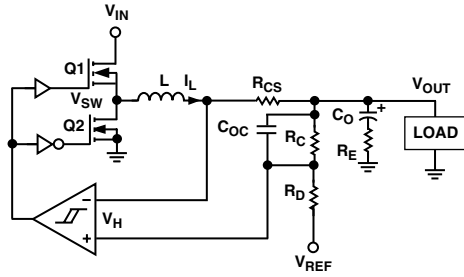
# ADP3203



*Figure 3. Modified Hysteretic Regulator with ADOPT*

The implementation requires adding a resistive divider ($R_C$ and $R_D$) between the reference voltage and the output and connecting the tap of the divider to the noninverting input of the hysteretic comparator. A capacitor, $C_{OC}$, is placed across the upper member ($R_C$) of the divider.

It is easily shown that the output impedance of the converter can be no less than the ESR of the output capacitor. A straightforward derivation demonstrates that the output impedance of the converter in Figure 3 can be minimized to equal the ESR, $R_E$, when the following two equations are valid (neglecting PCB trace resistance for now):

$$\frac{R_D}{R_C} = \frac{R_E - R_{CS}}{R_{CS}} \qquad (1)$$

and

$$C_{OC} = \frac{C_O R^2{}_E}{R_{CS} R_D} \qquad (2)$$

From Equation 2, the series resistance is:

$$R_{CS} = \frac{R_E}{1 + \dfrac{R_D}{R_C}} \qquad (3)$$

This is the ADOPT configuration and design procedure that allows the maximum possible ESR to be used while meeting a given load line specification.

It can be seen from Equation 3 that unless $R_D$ is zero or $R_C$ is infinite, $R_{CS}$ will always be smaller than $R_E$. An advantage of the circuit of Figure 3 is that if we select the ratio $R_D/R_C$ well above unity, the additional dissipation introduced by the series resistance $R_{CS}$ will be negligible. Another interesting feature of the circuit in Figure 3 is that the ac voltage across the two inputs of the hysteretic comparator is now equal only to the ac voltage across $R_{CS}$. This is due to the presence of the capacitor

$C_{OC}$, which effectively couples the ac component of the output voltage to the noninverting input voltage of the comparator. Since the comparator sees only the ac voltage across $R_{CS}$, in the circuit of Figure 3 the dependence of the switching frequency on the ESR of the output capacitor is completely eliminated. Equation 4 presents the expression for the switching frequency.

$$f = \frac{R_{CS}}{L V_H} \frac{(V_{IN} - V_{OUT}) V_{OUT}}{V_{IN}} \qquad (4)$$

**Multiphase Hysteretic Regulator with ADOPT**

Multiphase converters have very important advantages, including reduced rms current in the input filter capacitor (allowing the use of a smaller and less expensive device), distributed heat dissipation (reducing the hot-spot temperature and increasing reliability), higher total power capability, increased equivalent frequency without increased switching losses (allowing the use of a smaller equivalent inductances, and thereby shortening the load transient time), and reduced ripple current in the output capacitor (reducing the output ripple voltage and allowing the use of a smaller and less expensive output capacitor). Also, they have some disadvantages, which should be considered when choosing the number of phases. Those disadvantages include the need for more switches and output inductors than in a single-phase design (leading to a higher cost than a single-phase solution, at least below a certain power level), more complex control, and the possibility of uneven current sharing among the phases.

The family of ADP320x controllers alleviates two of the above disadvantages of multiphase converters. It presents a simple and cost-effective control solution and provides perfect current sharing among the phases. Figure 4 shows a simplified block diagram of a 3-phase converter using the control principle implemented with the ADP3203, the 3-phase member of the ADP320x family.

As Figure 4 shows, in the multiphase configuration the ripple current signal is multiplexed from all channels. During the on time of any given channel, its current is compared to the upper threshold of the hysteretic comparator. When the current reaches the upper threshold, the control FET of that channel is turned off. During the common off time of all channels, their currents are averaged and compared to the lower threshold. When the averaged channel current reaches the lower threshold, the hysteretic comparator changes state again and turns on the control FET of the next channel, as selected by the phase

splitter logic. This control concept ensures that the peak currents of all channels will be the same, and therefore the channel currents will be perfectly balanced. The ADOPT compensation can be used the same way as in the single-phase version discussed in the preceding text.

Since due to second order effects, the detailed design of a multiphase converter with the ADP320x family is rather complex, a design aid using MathSoft's MathCAD® program has been developed. Please contact ADI for further information.
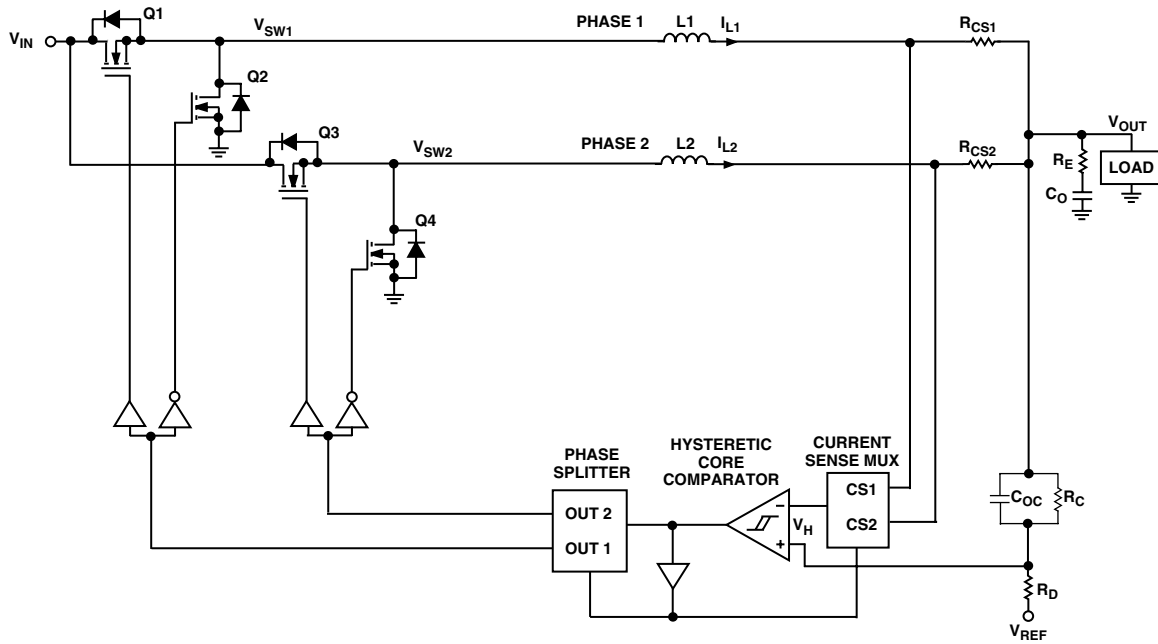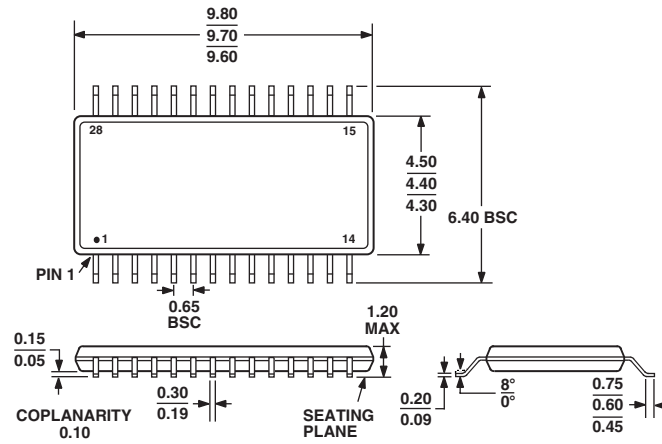


*Figure 4. 2-Phase Modified Hysteretic Regulator with ADOPT*

MathCAD is a registered trademark of MathSoft Engineering & Education, Inc.

## OUTLINE DIMENSIONS

### 28-Lead Thin Shrink Small Outline Package [TSSOP]
### (RU-28)
Dimensions shown in millimeters



**COMPLIANT TO JEDEC STANDARDS MO-153AE**

REV 0